KALI Technical Manual

This document covers the Technical Details of KALI

KALI RECLOCKER

The Kali takes the digital audio signals (I2S) from Sparky SBC or RPI through the on board FPGA based FIFO and does the re-clocking of the signal before sending it to the DAC. It produces jitter-less I2S then it feeds to the DAC boards **(Piano DAC or RPI compatible DAC boards.)**. Less information is lost, therefore better sound quality.

Two low phase noise crystal oscillators generate the Master clock. It provides accurate Master clock to DAC and FPGA. Component selection, Digital-Analog Partition and track layout have been in the forefront of our design to ensure noise immunity and best possible audio playback with the Kali.

Every SBC has a crystal that it used to send digital signals to your DACs. The accuracy of this crystal is very important in how well the DAC will transform the digital signal into analog sounds. Simply put: a better crystal means a better sound! Most SBCs use a very cheap crystal with lots of jitter in order to save costs.

Furthermore, there are 2 kinds of frequencies for digital files: 44.1Khz (wave files) and 48khz (streamed music). Some SBCs (like RPIs) can output only 48Khz, so imagine the degradation of the sound that was recorded at a different frequency.

Kali Will Solve Both of Those Problems: First, it has a very low jitter NDK crystal feed by LDOs in series for ultra quiet power supply. Second, the FPGA will read the incoming stream, will buffer the DATA 0.7s while discarding the incoming clocks. Using the NDKs it will reclock the buffered data OUTSIDE the fpga (since fpgas introduce about 200ps of jitter) and provide a MCLK/BCLK that is direct from crystal, providing a jitter-free (almost) to your DAC. Meanwhile, it will clock the file using the correct crystal (there are 2), fixing the problems stated above.

Features

- The basic design includes FPGA based FIFO board
- I2S input & output : 44.1 KHz, 48 KHz, 88.2 KHz, 96 KHz, 176.4 KHz, 192 KHz ,384 KHz - 16bit, 24bit or 32bit
- FIFO Memory: 4MB SRAM
- LED indicators (Power, Full, Lock, Empty, Sample Rate, Mclk)
- DC power supply: (5V/3A) with Filter circuits
- Multi-frequency output capability to support the full I2S working range from 44.1 KHz to 196 K
- Automatically switching frequencies according to the input I2S signals
- Extremely fast and very low propagation delay Flip-Flops are added on I2s signals
- output from FPGA, for synchronization with MCLK before sending to DAC
- Ultra-low-noise voltage regulators for optimal audio performance
- Integrated EEPROM for automatic configuration (with write-protection)

Tech Specs

- LED indicators (Power, Full, Lock, Empty, Sample Rate, Mclk)
- DC power supply: (5V/3A) with Filter circuits
- Operating Temperature Range is -25C to 85C
- The Kali board size: LWH = 58mm * 77.54mm * 23.8mm

TOP & BOTTOM VIEW

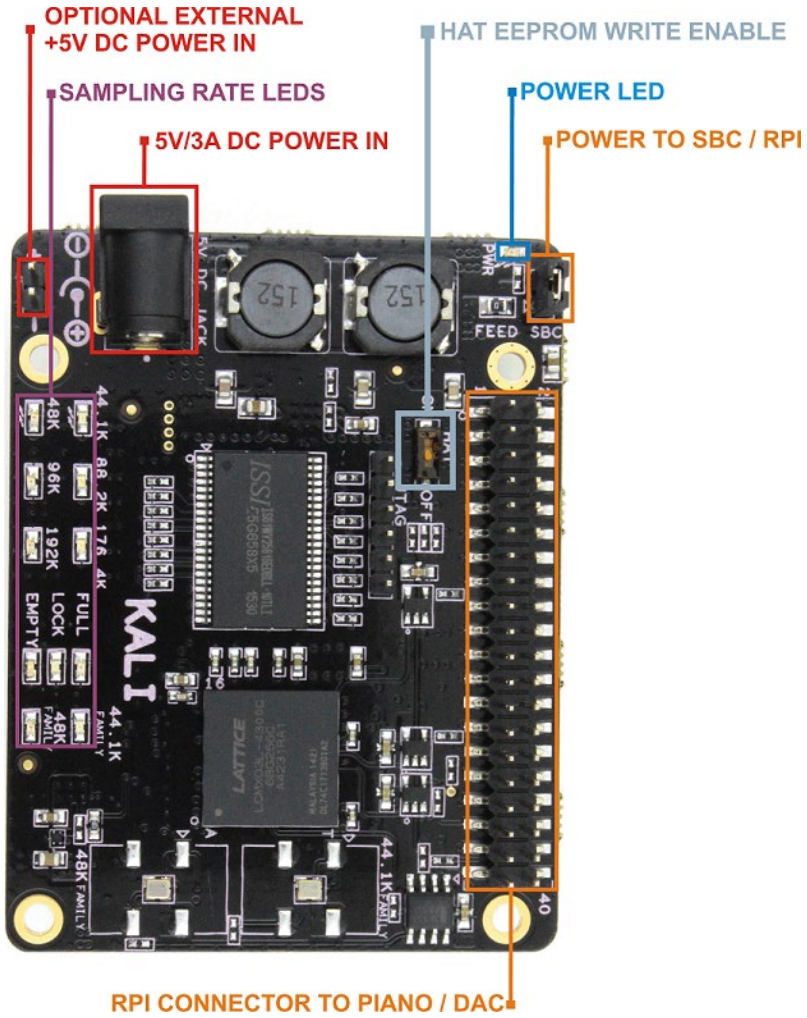


Fig 3: Top Side Kali

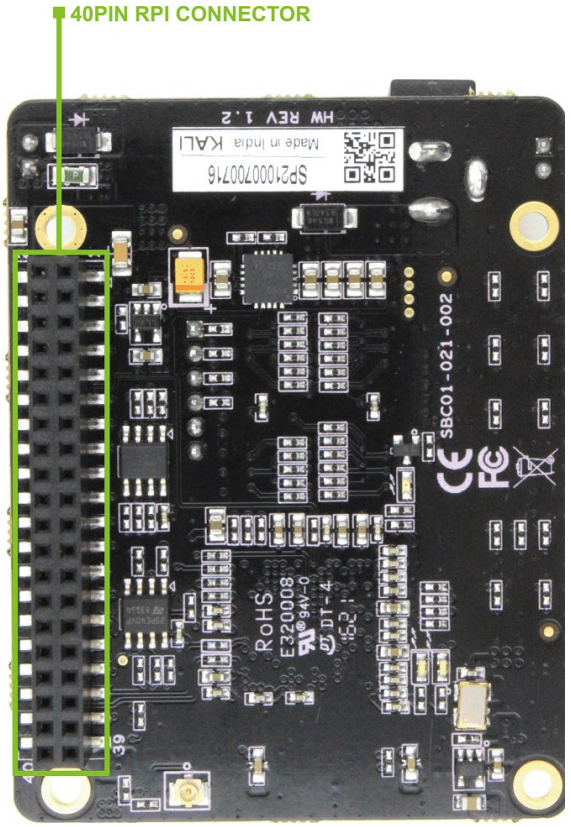


Fig 4: Bottom Side Kali

The Kali requires a +5 Volt power source to operate. Power should be applied to the 2.5mm DC JACK. This same power source only feeding to SBC (Sparky/RPI) and Piano/DAC boards.

WARNING: You need to power the KALI board when used with Sparky SBC or RPI Boards.

LED INDICATIONS

1) For Power up Indication - Green LED glow (refer fig)
2) While Playing 44.1K Family audio, respective sampling frequency & family LED (Blue) glows.
3) While Playing 48K Family audio, respective sampling frequency & family LED (Green) glows.
4) FIFO Status:

FULL- **Green** LED glows FIFO full.
LOCK - **Blue** LED glows FIFO locks to input sample rate.
EMPTY - **Red** LED When FIFO is empty.

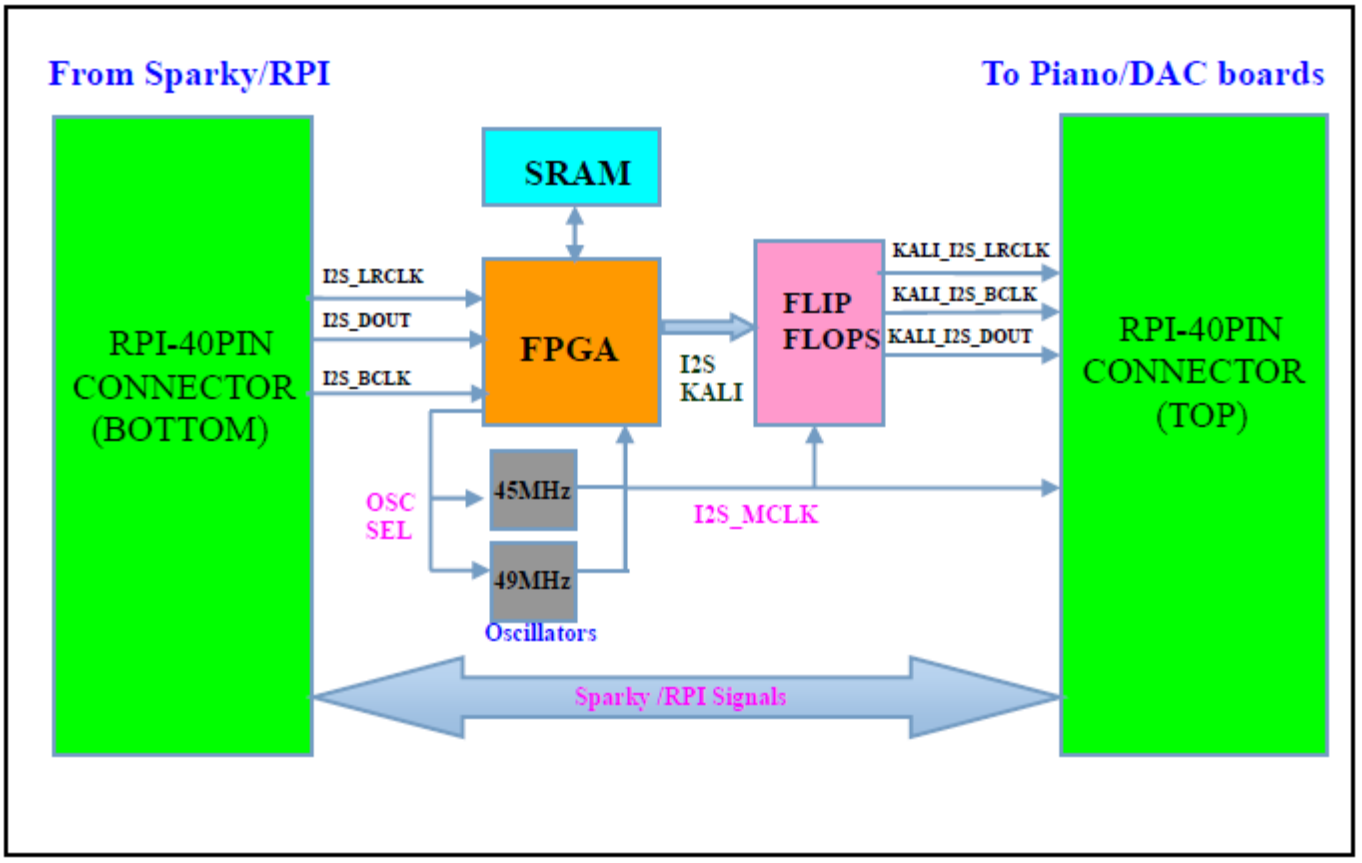
HAT Switch: change to ON position for HAT eeprom write protect disabling, OFF for enable (default state).

FEED SBC (POWER to SBC/RPI):
Default state U-LINK closed – SBC power through KALI BOARD
U-LINK OPEN – Power Isolation from SBC and KALI, need to connect individual power supply for SBC and KALI

Optional External +5V Power IN: Can feed +5VDC in through this header as per the polarity marking on board. This header provided for development testing purpose.

WARNING: Do not connect any jumper caps on this.

KALI BLOCK DIAGRAM



40 PIN BOTTOM CONNECTOR PIN OUT DETAILS

KALI 40 Pin Bottom connector (RPI compatible)					
RPI	Sparky signal	PIN	PIN	Sparky signal	RPI
NC	NC	1	2	DCIN +5V	DC +5V
SDA1-I2C	I2C -2 SDA	3	4	DCIN +5V	DC +5V
SCL1-I2C	I2C -2 SCLK	5	6	GND	GND
GPIO4	GPIOB14	7	8	UART5_TX	UART_TX
GND	GND	9	10	UART5_RX	UART_RX
GPIO17	GPIOB15	11	12	I2S_BCLK0	I2S_BCLK
GPIO27	GPIOB16	13	14	GND	GND
GPIO22	GPIOB17	15	16	GPIOB31	GPIO23
NC	NC	17	18	GPIOB30	GPIO24
SPI_MOSI	I2C-3 SDA/SPI0_MOSI	19	20	GND	GND
SPI_MISO	SPI0_MISO	21	22	GPIOB12	GPIO25
SPI_CLK	I2C -3 SCLK/SPIO_SCLK	23	24	SPIO_SS	GPIO8
GND	GND	25	26	SPDIF	GPIO7
ID_SD	I2C-1 SDA	27	28	I2C -1 SCLK	ID_SC
GPIO5	TP	29	30	GND	GND
GPIO6	GPIOB18	31	32	GPIOB3	GPIO12
GPIO13	GPIOB4	33	34	GND	GND
I2S_LRCLK	I2S_LRCLK0_2	35	36	GPIOB13	GPIO16
GPIO26	GPIOB19	37	38	I2S_DIN_2	I2S_DIN
GND	GND	39	40	I2S_DOUT_2	I2S_DOUT

40 PIN TOP CONNECTOR PIN OUT DETAILS

KALI 40 Pin TOP connector (RPI compatible)					
RPI	Sparky signal	PIN	PIN	Sparky signal	RPI
NC	NC	1	2	DCIN +5V	DC +5V
SDA1-I2C	I2C -2 SDA	3	4	DCIN +5V	DC +5V
SCL1-I2C	I2C -2 SCLK	5	6	GND	GND
GPIO4	GPIOB14	7	8	UART5_TX	UART_TX
GND	GND	9	10	UART5_RX	UART_RX
GPIO17	GPIOB15	11	12	KALI_BCLK	KALI_BCLK
GPIO27	GPIOB16	13	14	GND	GND
GPIO22	GPIOB17	15	16	GPIOB31	GPIO23
NC	NC	17	18	GPIOB30	GPIO24
SPI_MOSI	I2C-3 SDA/SPI0_MOSI	19	20	GND	GND
SPI_MISO	SPI0_MISO	21	22	GPIOB12	GPIO25
SPI_CLK	I2C -3 SCLK/SPIO_SCLK	23	24	SPIO_SS	GPIO8
GND	GND	25	26	SPDIF	GPIO7
ID_SD	I2C-1 SDA	27	28	I2C -1 SCLK	ID_SC
KALI_MCLK	KALI_MCLK	29	30	GND	GND
GPIO6	GPIOB18	31	32	GPIOB3	GPIO12
GPIO13	GPIOB4	33	34	GND	GND
KALI_LRCLK	KALI_LRCLK	35	36	GPIOB13	GPIO16
GPIO26	GPIOB19	37	38	I2S_DIN_2	I2S_DIN
GND	GND	39	40	KALI_DOUT	KALI_DOUT